Carter Cattadoris

carterjcattadoris@gmail.com | linkedin.com/in/cartercattadoris | github.com/CarterCattadoris

Education

Syracuse University, College of Engineering and Computer Science May 2027

Computer Engineering BS | GPA: 3.90 | Dean's List | ECS Leadership Scholar

Skills

Electrical Design: Hardware design, PCB design, PCB layout, circuit design, mixed-signal/analog front-ends, KiCad (schematic capture, hierarchical sheets, fabrication hand-off), electrical design and architecture, component selection, board bring-up, design verification, switching/linear power supplies, controlled-impedance routing, signal integrity, wiring harness design

Digital Logic & FPGA: VHDL, RTL/HDL design, Vivado, QuestaSim simulation, VLSI, FSM design, timing analysis

Embedded & Interfaces: Bare-metal ARM (ATSAMD21E18, STM32F030), ESP32-S3 (ESP-IDF/FreeRTOS), Teensy 4.1, RTOS, I2C/SPI/UART, CAN bus, microcontroller firmware, multi-domain board-level debug

Hardware Test & Validation: Vector network analyzer, spectrum analyzer, oscilloscope, signal generator, arbitrary waveform generator, power supplies, multimeter, S-parameter measurement, RF Tx/Rx characterization, impedance matching, low-noise measurement, test automation, troubleshooting, soldering, prototyping

Software & Scripting: C/C++, Python, MATLAB, Linux/Unix, Bash, Git version control

Work Experience

FPGA Engineering Intern May 2026 – Present

Lockheed Martin *Syracuse, NY*

- Designing a VHDL SPI interface to replace a legacy quad-IO, nibble-wide interface on an RFSoC-class platform, reducing pin count and routing complexity; verified behavior in simulation with QuestaSim

RF/Software Engineering Intern May 2025 – August 2025

Lockheed Martin *Syracuse, NY*

- Validated 100+ Tx/Rx modules with class-C high-power amplifiers, characterizing gain, S-parameters, and efficiency using signal generators, spectrum analyzers, and oscilloscopes across multiple frequency bands
- Built a C++ post-processing tool that parsed and distilled radar calibration data, turning raw measurement output into structured results for engineering analysis
- Characterized pulse droop and amplifier stability with arbitrary waveform generator and oscilloscope pairs, and reported module yield and failure-mode trends to program management

Projects

Technical Director / Electrical & Embedded Lead January 2025 – Present

Citrus Racing FSAE

- Driving a custom mixed-signal data-acquisition/telemetry PCB from blank-sheet architecture through schematic capture, component selection, and layout: an ESP32-S3 real-time core doubling as the wireless telemetry link, a dedicated analog acquisition front-end, a multi-rail power tree, and a GNSS receive chain integrated on one space-constrained board
- Defined the digital interface architecture, selecting components and pin assignments against real-time and signal-integrity needs: an ESP32-S3-master SPI bus shared by an ASM330LHHX IMU and an ADS7038-Q1 ADC digitizing the suspension-pot and additional analog sensor channels, a UART link to the GNSS receiver, and a CAN transceiver path bringing MoTeC M130 ECU data onto the ESP32-S3
- Engineered the GNSS receive chain from an SMA bulkhead to a u-blox NEO-M9N with bias-tee active-antenna power and hardware PPS time-stamping; hit the board's controlled-impedance targets—50 Ω CPWG for the RF, 90 Ω differential for USB—by sizing trace geometry to the fabricator's fixed stackup
- Laid out and integrated the power tree (LMR36015 400 kHz synchronous buck for the 3.3 V digital rail, TPS7A2030 low-noise LDO powering a separate analog island, P-channel MOSFET reverse-polarity and TVS input protection) for reliable operation under vibration and electrical noise
- Previously designed a Connector Hub PCB (LM2678 5 V / 5 A switching supply) and the full-vehicle wiring harness (mil-spec Tefzel, Deutsch DTM/Autosport), configured the MoTeC PDM30, and established the team's Git workflow for concurrent multi-developer KiCad work

Embedded Systems Engineer January 2026 – May 2026

Project ARGUS

- Developed real-time ESP32-S3 firmware in C (ESP-IDF/FreeRTOS) for an autonomous RC vehicle with mutex-protected multi-task state: a UDP listener parsing JSON motion commands feeding a 50 Hz motor-control task that drives a dual H-bridge via LEDC PWM
- Trained and deployed a YOLOv11n object-detection model on a Raspberry Pi 5 ground station, linking the vision pipeline to the vehicle over WiFi for autonomous tracking